ABSTRACT OF THE DISCLOSURE

An arithmetic unit includes a switching device 16 and a cache controller 19. The switching device 16 determines whether desired data to be read by the CPU 11 is in a RAM 14, and allows, depending on a result of the determination, the CPU 11 to directly read the desired data from a ROM 13. The cache controller 19 controls a cache 12 so that the RAM 14 is initialized based on cache data corresponding to the desired data stored in the cache 12. In an arithmetic unit having a CPU, a cache, RAM, and ROM configured in the above manner, the time required for a startup process is reduced.